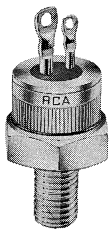
2N5441 2N5442
2N5444 2N5445

File No. 337

40-AMPERE SILICON TRIACS

Medium-Power, Gate-Controlled, Full-Wave Types

PRESS-FIT
2N5441 — 2N5442



STUD-MOUNTED
2N5444 — 2N5445

RCA-2N5441, 2N5442, 2N5444, and 2N5445* are gate-controlled, full-wave, silicon triacs. They are intended for the control of ac loads in applications such as heating controls, motor controls, arc welding equipment, light dimmers, and power switching systems.

These devices are designed to switch from an off-state to an on-state for either polarity of applied voltage with positive or negative triggering voltages to the gate.

Types 2N5441 and 2N5442 are press-fit types having an on-state current rating of 40 amperes at a case temperature of +70° C and repetitive off-state voltage ratings of 200 volts and 400 volts, respectively.

Types 2N5444 and 2N5445 are stud-mounted types having an on-state current rating of 40 amperes at a case temperature of +65° C and repetitive off-state voltage ratings of 200 volts and 400 volts, respectively.

* Formerly RCA Dev. Types TA2836, TA2837, TA2838, and TA2839, respectively.

Maximum Ratings, *Absolute-Maximum Values:*

For Operation with Sinusoidal Supply Voltage at Frequencies of 50/60 Hz, and with Resistive or Inductive Load

	2N5441 2N5444	2N5442 2N5445	
REPETITIVE PEAK OFF-STATE VOLTAGE*, V_{DROM}:			
Gate Open, For T_J = —65° to +110°C	200	400	V
RMS ON-STATE CURRENT, $I_{t(rms)}$			
For case temperature (T_C) of +65°C and a conduction angle of 360°C	40 (2N5444)	40 (2N5445)	A
For case temperature (T_C) of +70°C and a conduction angle of 360°C	40 (2N5441)	40 (2N5442)	A
PEAK SURGE (NON-REPETITIVE) ON-STATE CURRENT, I_{TSM}:			
For one full cycle of applied principal voltage	300	300	A
For more than one full cycle of applied voltage	See Fig. 6		
PEAK GATE-TRIGGER CURRENT†, I_{GTM}:			
For 10 μs max.	4	4	A
GATE POWER DISSIPATION:			
PEAK†, P_{GM} For 10 μs max. and $I_{GTM} \leq 4$ A peak	40	40	W
AVERAGE, $P_{G(AV)}$	0.75	0.75	W
TEMPERATURE RANGE ‡			
Storage	—65 to +150		°C
Operating (case)	—65 to +110		°C

* For either polarity of main terminal 2 voltage (V_{MT2}) with reference to main terminal 1.

† For either polarity of gate voltage (V_G) with reference to main terminal 1.

‡ For information on the reference point of temperature measurement, see *Dimensional Outlines.*

Features

- **5,000 Watt Control, 120-Volt Line Operation** } **2N5441, 2N5444**
- **10,000 Watt Control, 240-Volt Line Operation** } **2N5442, 2N5445**
- **40-A (rms) On-State Current Ratings**
- **300-A (Peak) Surge Full-Cycle Current Rating**
- **High dv/dt Capability**
- **Shorted-Emitter Design**
- **Center Gate Construction — Provides Rapid Gate Current Spreading, Faster Turn-On, and Minimum Temperature Effects**
- **Low Switching Losses**
- **Low On-State Voltage at High Current Levels**
- **Low Thermal Resistance**

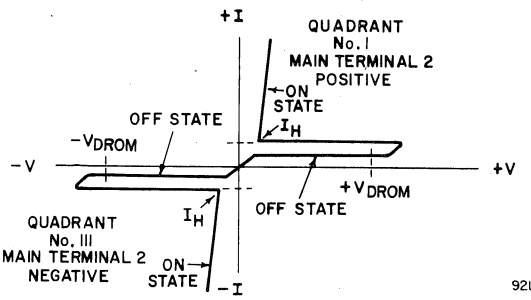


Fig. 1 - Principal Voltage-Current Characteristic.

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ELECTRICAL CHARACTERISTICS

Characteristics at Maximum Ratings (unless otherwise specified) and at Indicated Case Temperature (T_C).

For Definitions of Terms and Symbols, See Page 8.

CHARACTERISTICS	SYMBOL	LIMITS												UNITS
		2N5441			2N5442			2N5444			2N5445			
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
Peak Off-State Current:* Gate Open; At T_J = +110°C and V_{DROM} = Max. rated value	I_{DROM}	—	0.2	4	—	0.2	4	—	0.2	4	—	0.2	4	mA
Maximum On-State Voltage:* For i_T = 100A (peak) and T_C = +25°C	V_{TM}	—	1.7	2	—	1.7	2	—	1.7	2	—	1.7	2	V
DC Holding Current:* Gate Open; Initial principal current = 150mA (DC); At T_C = +25°C	I_{HO}	—	25	60	—	25	60	—	25	60	—	25	60	mA
For other case temperatures		← See Fig. 8. →												
Critical Rate of Rise of Commutation Voltage:* For $^vD = V_{DROM}$, $I_{t(rms)}$ = 40A, commutating di/dt = 22A/ms, and gate unenergized; At T_C = +65°C	dv/dt	—	—	—	—	—	—	5	30	—	5	30	—	V/μs
At T_C = +70°C		5	30	—	5	30	—	—	—	—	—	—	—	
Critical Rate of Rise of Off-State Voltage:* For $^vD = V_{RDOM}$, exponential voltage rise, and gate open; At T_C = +110°C	dv/dt	50	200	—	30	150	—	50	200	—	30	150	—	V/μs
DC Gate-Trigger Current:*† For ^vD = 12 volts (DC), R_L = 12Ω; T_C = +25°C, and Specified Triggering Mode:														
I+ Mode: V_{MT2} is positive, V_G is positive	I_{GT}	—	15	50	—	15	50	—	15	50	—	15	50	mA
III− Mode: V_{MT2} is negative, V_G is negative		—	20	50	—	20	50	—	20	50	—	20	50	
I− Mode: V_{MT2} is positive, V_G is negative		—	30	80	—	30	80	—	30	80	—	30	80	
III+ Mode: V_{MT2} is negative, V_G is positive		—	40	80	—	40	80	—	40	80	—	40	80	
For other case temperatures		← See Fig. 12 & 13. →												
DC Gate-Trigger Voltage:*† For ^vD = 12 volts (DC) and R_L = 12Ω; At T_C = +25°C	V_{GT}	—	1.35	2.5	—	1.35	2.5	—	1.35	2.5	—	1.35	2.5	V
For other case temperatures		← See Fig. 14. →												
For $^vD = V_{DROM}$ and R_L = 125Ω; At T_C = +110°C		0.2	—	—	0.2	—	—	0.2	—	—	0.2	—	—	
Gate-Controlled Turn-On Time: (Delay Time + Rise Time) For $^vD = V_{DROM}$ and I_{GT} = 120mA, 0.1 μs rise time, and i_T = 60A (peak); At T_C = +25°C	t_{gt}	—	3	—	—	3	—	—	3	—	—	3	—	μs
Thermal Resistance: Junction-to-Case	θ_{J-C}	—	—	0.8	—	—	0.8	—	—	0.9	—	—	0.9	°C/W
Transient		← See Fig. 15. →												

* For either polarity of main terminal 2 voltage (V_{MT2}) with reference to main terminal 1.

† For either polarity of gate voltage (V_G) with reference to main terminal 1.

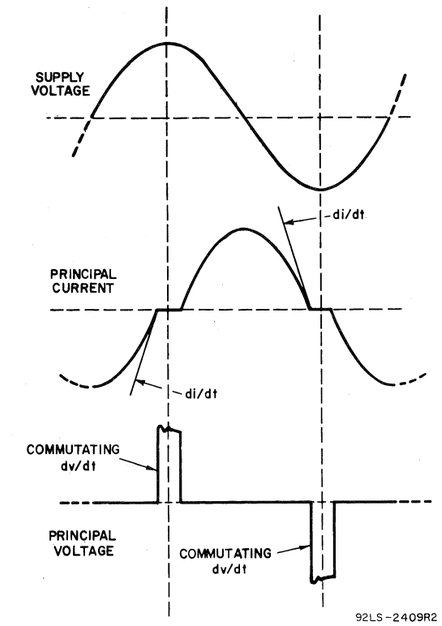


Fig. 2 - Oscilloscope Display of Commutating dv/dt.

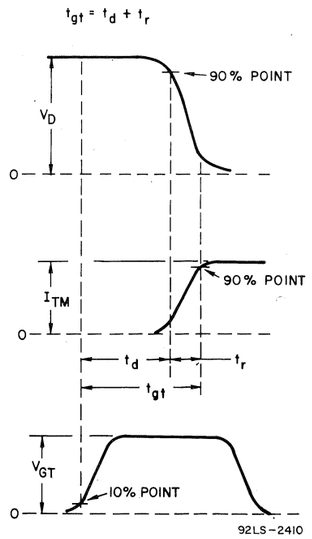


Fig. 3 - Oscilloscope Display for Measurement of Gate-Controlled Turn-On Time (t_{gt}) Test.

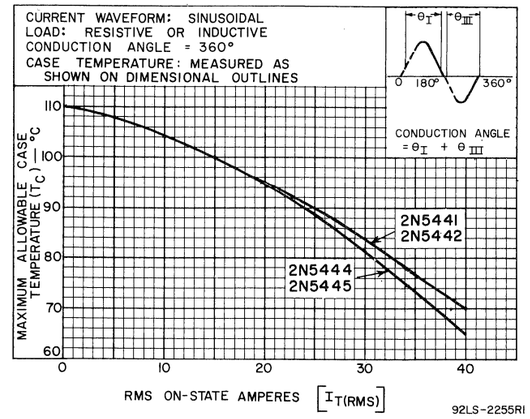


Fig. 4 - On-State Current Rating vs. Case Temperature.

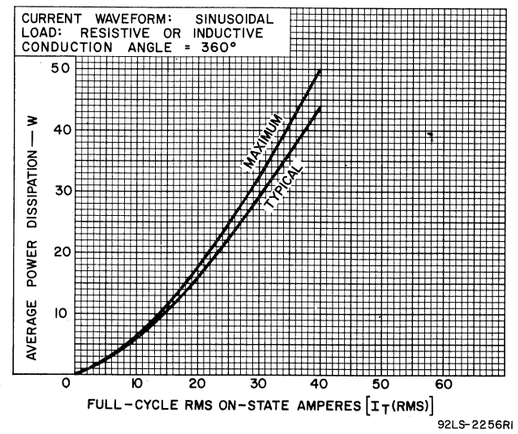


Fig. 5 - Power Dissipation vs. On-State Current.

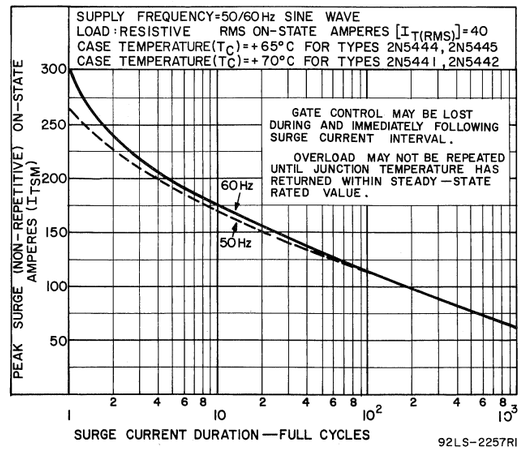

SUPPLY FREQUENCY=50/60Hz SINE WAVE
LOAD: RESISTIVE RMS ON-STATE AMPERES $[I_{T(RMS)}]$=40
CASE TEMPERATURE(T_C)=+65°C FOR TYPES 2N5444, 2N5445
CASE TEMPERATURE(T_C)=+70°C FOR TYPES 2N5441, 2N5442
PEAK SURGE (NON-REPETITIVE) ON-STATE AMPERES (I_{TSM})
300
250
200
150
100
50
GATE CONTROL MAY BE LOST DURING AND IMMEDIATELY FOLLOWING SURGE CURRENT INTERVAL.
OVERLOAD MAY NOT BE REPEATED UNTIL JUNCTION TEMPERATURE HAS RETURNED WITHIN STEADY-STATE RATED VALUE.
60Hz
50Hz
1 2 4 6 8 10 2 4 6 8 10^2 2 4 6 8 10^3
SURGE CURRENT DURATION—FULL CYCLES
92LS-2257RI

Fig. 6 - Peak Surge On-State Current vs. Surge Current Duration.

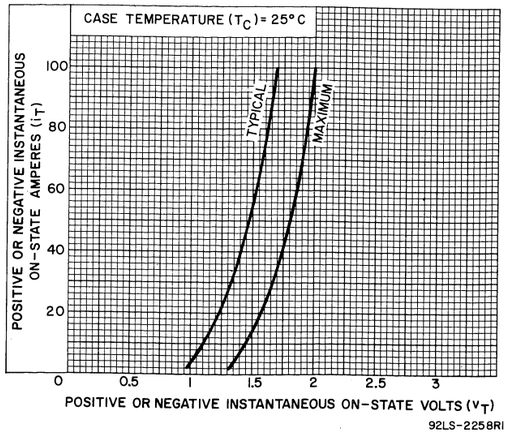


Fig. 7 - On-State Current vs. On-State Voltage.

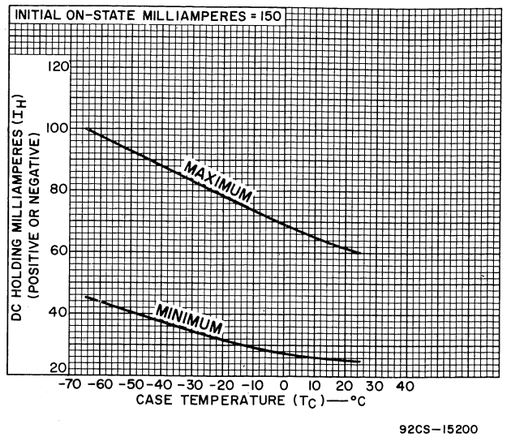


Fig. 8 - DC Holding Current Characteristics for Either Direction of On-State Current

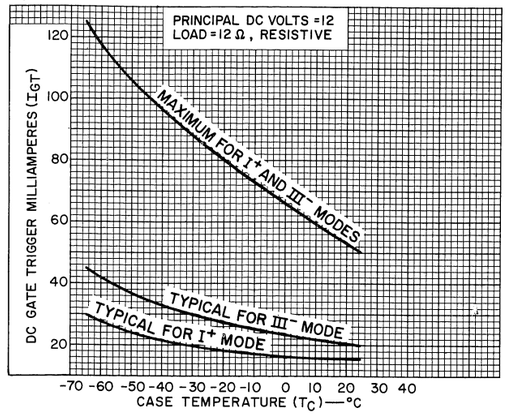

PRINCIPAL DC VOLTS = 12
LOAD = 12 Ω, RESISTIVE
MAXIMUM FOR I⁺ AND III⁻ MODES
TYPICAL FOR III⁻ MODE
TYPICAL FOR I⁺ MODE
DC GATE TRIGGER MILLIAMPERES (I_{GT})
CASE TEMPERATURE (T_C)—°C
92CS-15199

Fig. 12 - DC Gate-Trigger Currents for I⁺ and III⁻ Triggering Modes vs. Case Temperature.

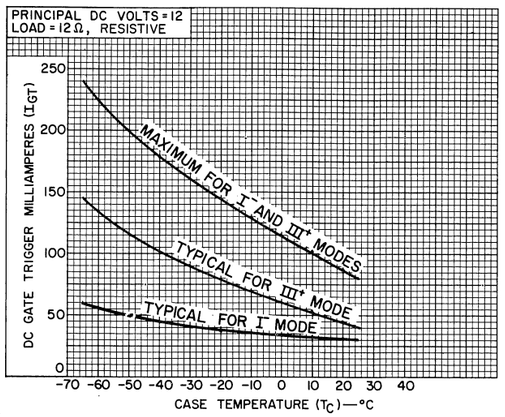

PRINCIPAL DC VOLTS = 12
LOAD = 12 Ω, RESISTIVE
MAXIMUM FOR I⁻ AND III⁺ MODES
TYPICAL FOR III⁺ MODE
TYPICAL FOR I⁻ MODE
DC GATE TRIGGER MILLIAMPERES (I_{GT})
CASE TEMPERATURE (T_C)—°C
92CS-15201

Fig. 13 - DC Gate-Trigger Currents for I⁻ and III⁺ Triggering Modes vs. Case Temperature.

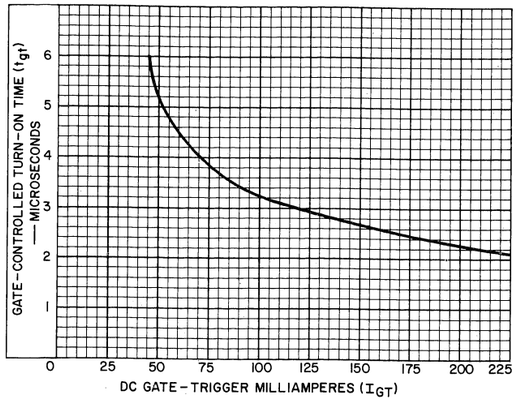


Fig. 9 - Typical Turn-On Time vs. Gate-Trigger Current.

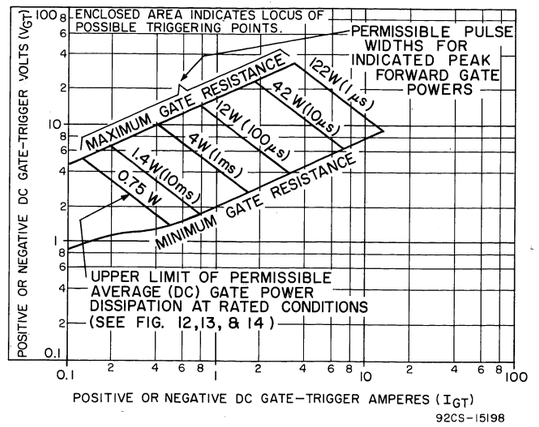

ENCLOSED AREA INDICATES LOCUS OF POSSIBLE TRIGGERING POINTS.
PERMISSIBLE PULSE WIDTHS FOR INDICATED PEAK FORWARD GATE POWERS
MAXIMUM GATE RESISTANCE
22W (1 μs)
12W (100 μs)
4.2W (10 μs)
4W (1ms)
1.4W (10ms)
0.75 W
MINIMUM GATE RESISTANCE
UPPER LIMIT OF PERMISSIBLE AVERAGE (DC) GATE POWER DISSIPATION AT RATED CONDITIONS (SEE FIG. 12,13, & 14)
POSITIVE OR NEGATIVE DC GATE-TRIGGER VOLTS (V_{GT})
POSITIVE OR NEGATIVE DC GATE-TRIGGER AMPERES (I_{GT})
92CS-15198

Fig. 10 - Gate Pulse Current Characteristics for All Triggering Modes.

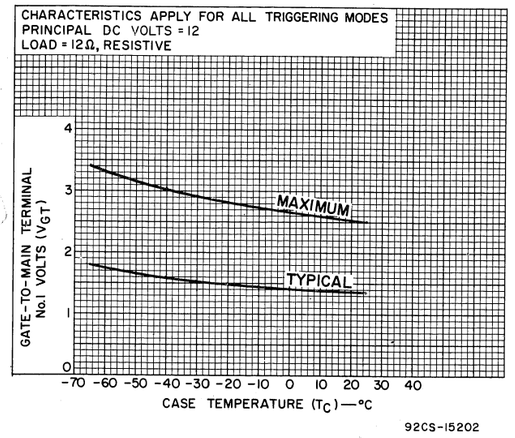


Fig. 14 - DC Gate-Trigger Voltage vs. Case Temperature.

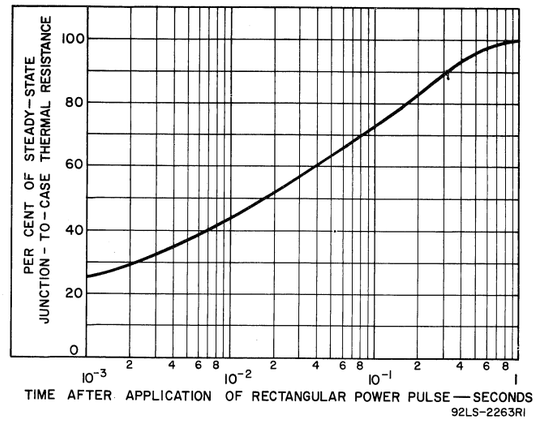
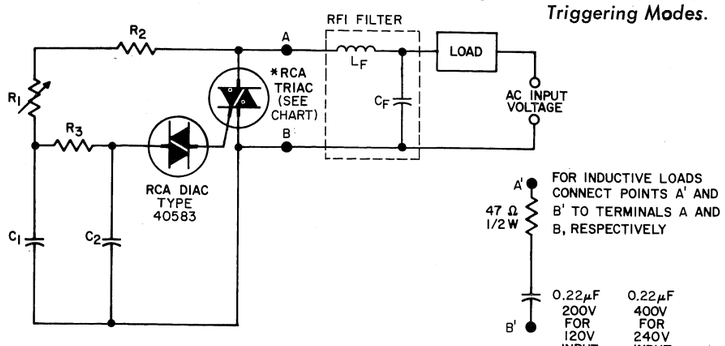

PER CENT OF STEADY-STATE JUNCTION - TO-CASE THERMAL RESISTANCE
TIME AFTER APPLICATION OF RECTANGULAR POWER PULSE—SECONDS
92LS-2263RI

Fig. 15 - Transient Thermal Resistance Variation vs. Time.



AC INPUT VOLTAGE	C_1	C_2	R_1	R_2	R_3	RFI FILTER L_F* (typ.)	RFI FILTER C_F* (typ.)	RCA TYPES
120V 60Hz	0.1μF 200V	0.1μF 100V	100KΩ 1/2W	1KΩ 1/2W	15KΩ 1/2W	100μH	0.1μF 200V	2N5441 2N5444
240V 50/60Hz	0.05μF 400V	0.1μF 100V	200KΩ 1/2W	7.5KΩ 2W	7.5KΩ 2W	100μH	0.1μF 400V	2N5442 2N5445

*Typical values for lamp dimming circuits.

Fig. 11 - Typical Phase-Control Circuit for Lamp Dimming, Heat Controls, and Universal Motor Speed Controls.

TYPE	MOUNTING ARRANGEMENT	THERMAL RESISTANCE (Case-to-Heat Sink)
2N5441 2N5442	Pressed into heat sink. (Minimum required thickness of heat sink = 1/8 in.)	0.5°C/W
	Soldered directly to heat sink. (60-40 solder with a melting point of 188°C is recommended. Exposure time should be sufficient to cause solder to flow freely).	0.1 to 0.35°C/W
2N5444 2N5445	Directly mounted on heat sink with or without the use of heat sink compound.	0.6°C/W
	Mounted on heat sink with a 0.004" to 0.006" (.10 to .15 MM) thick mica insulating washer (between unit and heat sink).	
	Without heat sink compound	2.5°C/W
	With heat sink compound	1.5°C/W

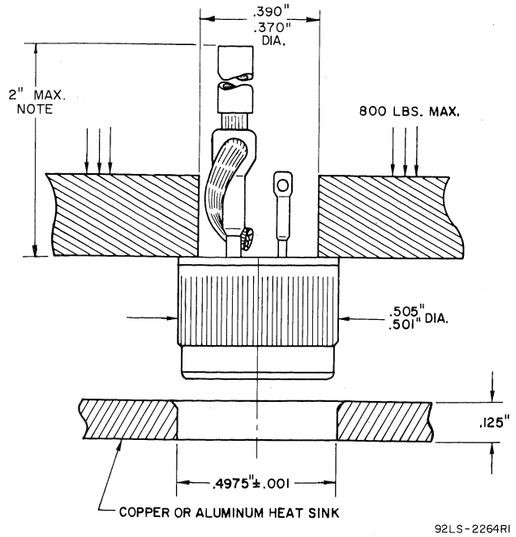
Table 1 - Case-to-Heat Sink Thermal Resistance for Recommended Mounting Arrangements

MOUNTING CONSIDERATIONS

Press-fit mounting of the 2N5441 and 2N5442 depends upon an interference fit between the thyristor case and the heat sink. As the thyristor is forced into the heat-sink hole, metal from the heat sink flows into the knurl voids of the thyristor case, and thereby provides an intimate contact between the heat sink and the thyristor case that is mechanically, thermally and electrically secure.

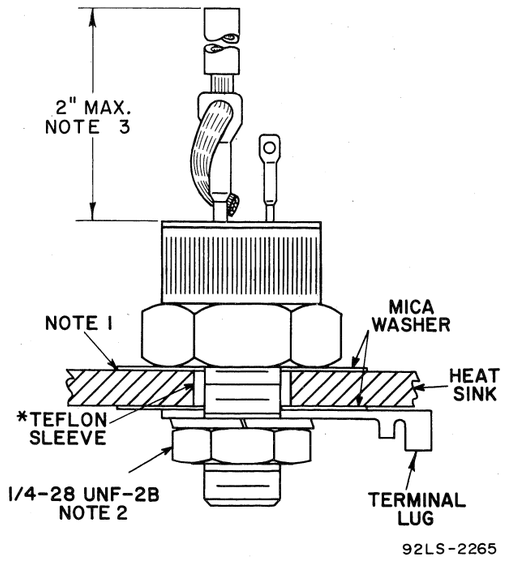
A recommended mounting method, shown in Fig. 16, shows press-fit knurl and heat-sink hole dimensions. If these dimensions are maintained, a "worst-case" condition of 0.0085 in. interference fit will allow press-fit insertion below the maximum allowable insertion force of 800 pounds. A slight chamfer in the heat-sink hole will help center and guide the press-fit package properly into the heat sink. The insertion tool should be a hollow shaft having an inner diameter of 0.380 ± 0.010 in. and an outer diameter of 0.500 in. These dimensions provide sufficient clearance for the leads and assure that no direct force is applied to the glass seal of the thyristor.

The press-fit package is not restricted to a single mounting arrangement; direct soldering and the use of epoxy adhesives have been successfully employed. The press-fit case is tin-plated to facilitate direct soldering to the heat sink. A 60-40 solder should be used and heat should only be applied long enough to allow the solder to flow freely.



Note: It is recommended that No. 12 stranded wire, 2 in. long, be connected to main terminal 1 when these triacs are operated at the full on-state current rating of 40 amperes.

Fig. 16 - Suggested Mounting Arrangement for Press-Fit Types 2N5441 & 2N5442



Note 1: Dow Corning 340 silicon heat-sink compound, or equivalent.

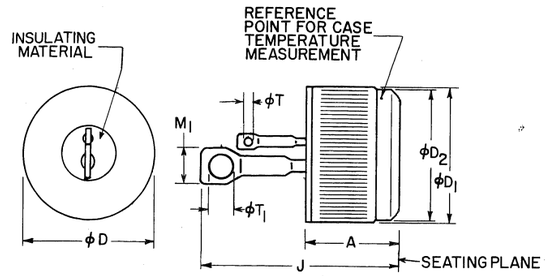
Note 2: The recommended torque is 26 to 36 inch-pounds applied to a 1/4-28 UNF-2B hex nut assembled on thread. The applied torque during installation should not exceed 50 inch-pounds.

Note 3: It is recommended that No. 12 stranded wire, 2 in. long, be connected to main terminal 1 when these triacs are operated at the full on-state current rating of 40 amperes.

* Trademark: E. I. DU PONT DE NEMOURS & CO. INC.

Fig 17 - Suggested Mounting Arrangement for Stud Types 2N5444 & 2N5445

DIMENSIONAL OUTLINE FOR TYPES 2N5441 & 2N5442

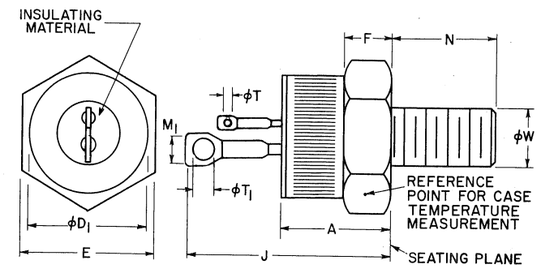


SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	—	.380	—	9.65	
ϕD	.501	.510	12.73	12.95	
ϕD_1	—	.505	—	12.83	2
ϕD_2	.465	.475	11.81	12.07	
J	—	1.045	—	26.54	
M_1	.210	.300	5.33	7.62	1
ϕT	.058	.068	1.47	1.73	
ϕT_1	.125	.165	3.18	4.19	

NOTES:
1. Contour and angular orientation of these terminals is optional.
2. Outer diameter of knurled surface.

92CS-15207

DIMENSIONAL OUTLINE FOR TYPES 2N5444 & 2N5445



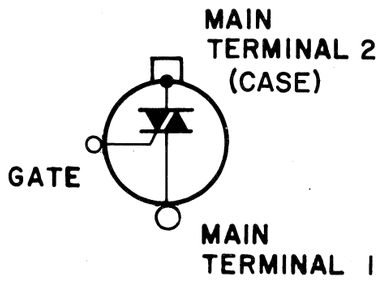
Note 1: 1/4-28 UNF-2A. Maximum pitch dia. of plated threads shall be basic pitch dia. 0.2268", minimum pitch dia. 0.2225", Ref. (Screw Thread Standards for Federal Services 1957) Handbook H28 1957 P1.

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	.330	.505	8.4	12.8	—
ϕD_1	—	.544	—	13.81	—
E	.544	.562	13.82	14.28	—
F	.113	.200	2.87	5.08	3
J	—	1.193	—	30.30	—
M_1	.210	.300	5.34	7.62	1
N	.422	.453	10.72	11.50	—
ϕT	.058	.068	1.47	1.73	—
ϕT_1	.125	.165	3.18	4.19	—
ϕW	.2225	.2268	5.652	5.760	2

NOTES:
1. Contour and angular orientation of these terminals is optional.
2. Pitch diameter of 1/4-28 UNF-2A (coated) threads (ASA B1.1-1960).
3. A chamfer or undercut on one or both ends of hexagonal portion is optional.

92CS-15208

TERMINAL CONNECTIONS



Long Terminal — Main Terminal 1

Short Terminal — Gate

Case — Main Terminal 2

DEFINITIONS OF TERMS AND SYMBOLS

These terms and symbols follow the latest recommended standards of JEDEC. For convenience, formerly used symbols have been cross-referenced to the new standards.

PRINCIPAL VOLTAGE DEFINITIONS

Repetitive Peak Off-State Voltage — V_{DROM} (Formerly V_{BOM}) — The maximum instantaneous value of principal off-state voltage which may be applied to the thyristor, including all repetitive transient voltages, which will not switch the thyristor from the off-state to the on-state with the gate open and at specified conditions of thyristor junction temperature.

Instantaneous Off-State Voltage — ^{V}D (Formerly ^{V}BX) — The instantaneous value of principal voltage, positive or negative, applied between main terminals 1 and 2 when the thyristor is in the off-state.

Instantaneous On-State Voltage — ^{V}T (Formerly ^{V}AA) — The instantaneous value of principal voltage, positive or negative, when the thyristor is in the on-state at a given instantaneous current.

Critical Rate of Rise of Off-State Voltage — Critical dv/dt — The value of the exponential rate of rise of principal voltage below which switching from the off-state to the on-state will not occur, and above which switching may occur, under specified conditions. This rate of rise is defined as follows:

$$dv/dt = \frac{0.63\ V_{DROM}}{t}$$

where t is the time required for the principal voltage to rise from zero to 0.63 of V_{DROM}.

Critical Rate of Applied Commutating Voltage — Commutating dv/dt — The instantaneous rate of rise of principal voltage occurring during commutation which will not cause the thyristor to switch to the on-state under specified conditions.

PRINCIPAL CURRENT DEFINITIONS

RMS On-State Current — $I_{T(RMS)}$ (Formerly I_{ON}) — The RMS value of the principal current when the thyristor is in the on-state.

Instantaneous On-State Current — i_T (Formerly i_{AA}) — The instantaneous value of principal current when the thyristor is in the on-state.

Peak Surge (Non-Repetitive) On-State Current — I_{TSM} (Formerly i_{SM}) — An overload on-state current of specific time duration, and peak value, which may be conducted through the thyristor for one full cycle from a 60-Hz supply in a single-phase circuit with a resistive load. The thyristor shall be operating within its specified operating voltage, RMS current, gate power, and temperature ratings prior to the surge current. The surge current may be repeated after sufficient time has elapsed for the device to return to pre-surge thermal equilibrium conditions.

Peak Off-State Current — I_{DROM} (Formerly I_{BOM}) — The current which flows through the main terminals when the thyristor is in the off-state and when the principal voltage is V_{DROM} under specified conditions of junction temperature and with the gate open.

DC Holding Current — I_H (Formerly I_{HOX}) — The principal current required to maintain the thyristor in the on-state for a specified temperature.

GATE DEFINITIONS

DC Gate-Trigger Current — I_{GT} — The gate current which will switch a thyristor from the off-state to the on-state under specified conditions of principal voltage and case temperature.

DC Gate-Trigger Voltage — V_{GT} — The gate voltage required to produce the gate-trigger current necessary to switch a thyristor from the off-state to the on-state for specified conditions of principal voltage and case temperature.

Peak Gate-Trigger Current — I_{GTM} — The maximum gate-trigger current, positive or negative, which is allowed in switching a thyristor from the off-state to the on-state for a specified time duration.

Peak Gate Power Dissipation — P_{GM} — The maximum power which may be dissipated between the gate and main terminal 1 for a specified time duration.

Average Gate Power Dissipation — $P_{G(AV)}$ — The value of gate power which may be dissipated between the gate and main terminal 1 averaged over a full cycle.

MISCELLANEOUS

Principal Voltage is the voltage between the main terminals. The principal voltage is called positive when the potential of main terminal 2 is higher than the potential of main terminal 1.

Principal Current is the current that flows through the main terminals.

Gate-Controlled Turn-On Time — t_{gt} (Formerly t_{on}) — The time interval between the 10 per-cent point at the beginning of the gate-trigger voltage pulse and the instant when the principal current has risen to the 90 per-cent point of its peak voltage during switching of the thyristor from the off-state to the on-state by a gate pulse.

Load Resistance — R_L — The value of fixed resistance connected in series with a main terminal of the thyristor and the power source.

Thermal Resistance, Junction to Case — $\theta_{J\text{-}C}$ — The temperature difference between the thyristor junction and the thyristor case divided by the power dissipation causing the temperature difference under conditions of thermal equilibrium.

For basic thyristor theory, circuits, and application information on Triacs, refer to "RCA Silicon Power Circuits Manual," SP-50.

RCA Application Notes on Thyristors (Triacs)

AN-3697 *"Triac Power Control Applications," by J. V. Yonushka*

AN-7347 *"Use of Triacs in Light-Dimmer Applications" by J. M. Nielson*

Single copies of these Application Notes are available on request from RCA, Commercial Engineering, Building GM-1, Harrison, N.J. 07029